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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Shibly S. Ahmed et al.	)	Group Art Unit: 2815
	)	
Application No.: 10/614,001	)	Examiner: J. Fenty
	)	
Filed: July 8, 2003	)	
	)	
For: SELECTIVE SILICIDATION OF GATES IN SEMICONDUCTOR DEVICES TO ACHIEVE MULTIPLE THRESHOLD VOLTAGES	)	

TRANSMITTAL FOR APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Appeal Brief-Patents
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Transmitted herewith is an Appeal Brief in support of the Notice of Appeal filed December 1, 2004.

Enclosed is a check for ☐ $250.00 ☒ $500.00 to cover the Government fee.

The Commissioner is hereby authorized to charge any other appropriate fees that may be required by this paper that are not accounted for above, and to credit any overpayment, to Deposit Account No. 50-1070.

Respectfully submitted,

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Date: February 1, 2005

PATENT
Attorney Docket No. H1484

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

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Customer Window, Mail Stop Appeal Brief – Patents
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

This Appeal Brief is submitted in response to the rejection mailed September 24, 2004 and in support of the Notice of Appeal filed December 1, 2004.

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-7, 14-19 and 21-23 are pending in this application and have been rejected. Claims 8-13 and 20 have been previously canceled without prejudice or disclaimer. Claims 1-7, 14-19 and 21-23 are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the Office Action mailed September 24, 2004.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Each of the independent claims involved in this appeal is recited below, followed in parenthesis by examples of where support can be found in the specification and drawings for the claimed subject matter. In addition, each dependent claim argued separately below is also summarized below in a similar manner.

Claim 1 recites a semiconductor device, comprising: a substrate (Fig.1, 110); an insulating layer formed on the substrate (page 5 paragraph 26, Fig. 1, 120); a first device (Fig. 5A, 100) formed on the insulating layer, including: a first fin (Fig. 5A, 210) formed on the insulating layer, and a first silicided gate (Fig. 6, 600) formed over a portion of the first fin and including a first thickness of silicide material (page 9, paragraphs 42-43); and a second device (Fig. 7, 100') formed on the insulating layer, including: a second fin (Fig. 8, 210)

formed on the insulating layer, and a second silicided gate (Fig. 7, 700) formed over a portion of the second fin and including a second thickness of silicide material different from the first thickness (page 10, paragraphs 45-46), wherein a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device (page 10, paragraph 47).

Claim 14 recites a semiconductor device, comprising: a substrate (Fig. 1, 110); an insulating layer formed on the substrate (Fig. 1, 120); a first device formed on the insulating layer (Fig. 5A, 100), including: a first fin formed on the insulating layer (Fig. 5A, 210), a first dielectric layer formed on the first fin (pages 6-7, paragraph 32, Fig. 2B, 140), and a partially silicided gate formed over a portion of the first fin and the first dielectric layer (page 9, paragraph 42, Fig. 6, 600); and a second device formed on the insulating layer (Fig. 7, 100'), including: a second fin formed on the insulating layer (Fig. 8, 210), a second dielectric layer formed on the second fin (Fig. 7, 140), and a fully silicided gate formed over a portion of the second fin and the second dielectric layer (page 10, paragraphs 45-46, Fig. 7, 700), wherein a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device (page 10, paragraph 47).

Claim 4 recites that the second silicided gate is fully silicided (page 10, paragraph 45 and Fig. 7, 700).

Claim 19 recites that the semiconductor device of claim 14, further comprises: a third device formed on the insulating layer, including: a third fin formed on the insulating layer, a third dielectric layer formed on the third fin, and a partially silicided gate formed over a portion of the third fin and the third dielectric layer (Fig. 8, 100''), wherein a silicided portion of the partially silicided gate formed over the portion of the third fin and the third dielectric layer has a different thickness than a silicided portion of the partially silicided gate formed over the portion of the first fin and the first dielectric layer (pages 10-11, paragraph 48 and Fig. 8).

Claim 21 recites the semiconductor device of claim 1, wherein a width of the first fin and the second fin ranges from about 10 Å to about 100 Å (pages 6-7, paragraph 32).

Claim 22 recites the semiconductor device of claim 14, wherein a width of the first fin and the second fin ranges from about 10 Å to about 100 Å (pages 6-7, paragraph 32).

Claim 23 recites the semiconductor device of claim 18, wherein a drain region of the first fin is electrically connected to a source region of the second fin (page 11, paragraph 50).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-7, 14-18 and 21-23 have been rejected under 35 U.S.C. § 103(a) as being

unpatentable over Fried et al. (U.S. Patent No. 6,657,259; hereinafter Fried) in view of Wang et al. (U.S. Patent No. 6,589,836; hereinafter Wang) and further in view of Dash et al. (U.S. Patent No. 4,399,605) and Moslehi (U.S. Patent No. 5,397,909).

B. Claim 19 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fried in view of Wang and further in view of Takeda et al. (U.S. Patent Publication No. 2001/0045589; hereinafter Takeda).

VII. ARGUMENT

A. Rejection under 35 U.S.C. § 103 based on Fried in view of Wang and further in view of Dash and Moslehi

1. Claims 1-3, 6 and 7

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an

applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

With these principles in mind, claim 1 recites a semiconductor device that includes a first device and a second device formed on an insulating layer. The first device includes a first fin formed on the insulating layer and a first silicided gate formed over a portion of the first fin, where the first silicided gate includes a first thickness of silicide material. The second device includes a second fin formed on the insulating layer and a second silicided gate formed over a portion of the second fin, where the second silicided gate includes a second thickness of silicide material different from the first thickness. Claim 1 further recites that a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.

The Final Office Action states that Fried discloses a semiconductor device including a

first and second device that include a fin 206 and a silicided gate 212 and points to Fig. 7B and col. 10, lines 7-8 for support (Final Office Action – page 2). The Final Office Action admits that Fried does not disclose that silicide regions 212 have different thicknesses (Final Office Action – page 2). The Final Office Action, however, states that Wang discloses thin and thick silicide layers (15b and 15c) on top of gate structures 6 and points to Fig. 7 for support (Final Office Action – page 2). The Final Office Action further states a threshold voltage of the second device (apparently of Wang) varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device (Final Office Action – page 3). The Final Office Action further points to Dash at col. 4, lines 41-46 and Lund et al. (U.S. Patent No. 4,319,395; hereinafter Lund) at col. 5, line 65 to col. 6, line 2 as allegedly supporting the notion that the claimed values are an inherent characteristic of the claimed material. Appellants respectfully disagree.

Initially, Appellants note that it is not clear as to whether the Final Office Action is using an inherency rational with respect to the claimed threshold voltage of the second device with respect to the first device or an obviousness-type rationale since footnote 1 at pages 3 and 4 appears to be contradictory, as discussed below. In either case, Appellants respectfully submit that none of the references of record, either singly or in combination, inherently discloses or suggests that a threshold voltage of a second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of a first device, as required by claim 1.

For example, the Final Office Action admits that Wang does not disclose this feature, but states that although empirical values are not given, "the claimed values are an inherent

characteristic of the material and do not represent values that could not have been obtained through routine experimentation" (Final Office Action - pages 3-4 at footnote 1). First, footnote 1 is contradictory. That is, footnote 1 indicates that the claimed values are an "inherent characteristic," but then states that the values do not represent values that could not have been obtained through "routine experimentation" and therefore, "the cited art is adequate to reject the claim."

Appellants assert that the claimed range is clearly not an inherent characteristic of Wang. That is, the threshold voltage of the device in region 2 of Fig. 7 of Wang does not necessarily vary about 200 millivolts to about 400 millivolts from the threshold voltage of the device in region 1 of Wang. Appellants further submit that the Examiner's statement with respect to "routine experimentation" also clearly indicates that Wang cannot be construed as inherently disclosing this feature of claim 1.

The Final Office Action, however, points to Dash at col. 4, lines 41-46 and Lund at col. 5, line 65 to col. 6, line 2 as allegedly supporting the notion that the claimed values are obvious (footnote 1 at page 3). Appellants respectfully disagree.

Dash at col. 4, lines 41-46 discloses that a platinum silicide gate electrode 50 is used effectively as both an ion implant barrier and as a high work function material for controlling the magnitude of the threshold voltage of the P-channel transistor. Lund at col. 5, line 65 to col. 6, line 2 discloses that the work function is one of the determinant factors in establishing the threshold voltage of the device and that without doping the polycrystalline silicon with boron, the subsequent formation of platinum silicide would result in a p-channel device having

too high a threshold voltage.

It is not clear how these general discussions regarding using silicide gate electrodes to control the threshold voltage can be construed to suggest that the specifically claimed feature recited in claim 1 is somehow obvious. That is, the portions of Dash and Lund relied upon as supporting the notion that the claimed threshold voltage of the second device relative to the first device recited in claim 1 is obvious merely discloses that the threshold voltage of a device may be controlled, in part, by the material in the gate. Appellants, however, are not generally claiming that the material in the gate affects the threshold voltage of the device. Appellants are specifically claiming that a threshold voltage of a second device varies about 200 millivolts to about 400 millivolts from the threshold voltage of a first device. A general disclosure that the material in a gate affects the threshold voltage of a device cannot be fairly construed to suggest that the claimed threshold voltage of a second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of a first device formed on the same semiconductor device, as required by claim 1. In this respect, Appellants rely upon In re Deuel, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995), wherein it was held that generalizations do not establish the realistic motivation to modify a specific reference in a specific manner to arrive at a specifically claimed invention.

The Final Office Action also states that the claimed values "do not represent values that could not have been obtained through routine experimentation." This statement clearly indicates that none of the four references inherently discloses the claimed feature. This statement, however, indicates that the Examiner believes that the claimed range would have

somehow been obtained through routine experimentation. Appellants strongly disagree.

None of the four references even mentions any particular values with respect to varying a threshold voltage of one device with respect to a second device, much less that a threshold voltage of second device located on the same semiconductor device as a first device varies about 200 to 400 millivolts from the threshold voltage of the first device. Such speculation regarding routine experimentation, with not even any one of the references indicating any particular values with respect to threshold voltages of one device with respect to another device, does not meet the requirements of 35 U.S.C. § 103.

Further, in the Response to Argument section, the Final Office Action states that Appellants' disclosure at paragraph 50 supports the Examiner's interpretation of the prior art (Final Office Action – page 7). Appellants respectfully disagree.

Appellants' disclosure at paragraph 50 states that two FinFET devices within the same circuit element may achieve different threshold voltages by using gate structures 600 and 700 that have different silicide thicknesses. Once again, Appellants are not claiming that different thicknesses of silicide will result in different threshold voltages. Appellants are specifically claiming that a threshold voltage of a second device varies about 200 millivolts to about 400 millivolts from the threshold voltage of a first device formed on the same semiconductor device. None of the prior art discloses or suggest this feature and Appellants' own disclosure clearly provides no support for the argument that such a feature is obvious or can be obtained through routine experimentation, absent impermissible hindsight.

In addition, even if, for the sake or argument, the combination of Fried, Wang, Dash

and Lund could be fairly construed to disclose or suggest each of the features of claim 1, Appellants submit that the motivation relied upon for combining these four references does not satisfy the requirements of 35 U.S.C. § 103.

For example, Appellants note that Fried is directed to multiple-plane FinFET complementary metal oxide semiconductor (CMOS) devices (Fried – col. 1, lines 6-8). Wang is directed to a method for forming a thin salicide on elements of a P channel metal oxide semiconductor (PMOS) device, while simultaneously forming thicker salicide on elements of an N channel metal oxide semiconductor (NMOS) device (Wang – col. 1, lines 9-14). Appellants submit that it would not have been obvious to combine the teachings of Fried and Wang.

For example, the Final Office Action states that it would have been obvious to combine these references "for the purpose, for example, of diversifying the device by varying the resistance of the gate layers" and points to Wang at col. 4, lines 54-57 for support (Final Office Action – pages 2-3). Appellants respectfully disagree.

Wang at col. 4, lines 54-57 discloses that robust metal silicide layer 15c on gate structure 6 will result in a desired low resistance Rs for the narrow gate structure, allowing the desired NMOS performance to be realized. This portion of Wang provides no support for modifying Fried to include this feature of Wang. That is, this portion of Wang relied upon as allegedly providing motivation for the combination merely discloses that metal silicide layer 15c reduces the resistivity of the gate structure. The alleged motivation, therefore, is merely a conclusory statement regarding an alleged benefit of combining a feature of Wang with Fried.

Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

In addition, Appellants note that Dash has been used in the grounds of rejection at paragraph 1 along with Moslehi (Final Office Action – page 2). Moslehi, however, has not been used in any portion of the rejection. Appellants assume that the Examiner intended to include Lund in the grounds of rejection since Lund was referenced at footnote 1 of the Final Office Action. In any event, the Final Office Action has not provided any statement as to why it would have been obvious to combine features from Dash and Lund with the combination of Fried and Wang. Therefore, a prima facie case of obviousness with respect to claim 1 has not been made.

Further, Appellants assert that it would not have been obvious to combine features from Dash and Lund with the combination of Fried and Wang absent impermissible hindsight. That is, Dash is directed to a method of making dense complementary transistors (Dash – Abstract) and Lund is directed to making a self-aligned MOS transistor (Lund – Abstract). These references are essentially unrelated to Fried and Wang, other than the fact that all may involve semiconductor devices. The mere fact that one or more references allegedly provide a missing teaching with respect to a claim does not provide objective motivation as to why it would have been obvious to combine various references.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 1 under 35 U.S.C. § 103 based on Fried, Wang, Dash and Lund (and Moslehi) is improper. Accordingly, reversal of the rejection of claims 1-3, 6 and 7 is respectfully requested.

2. Claims 4, 5 and 14-18

Claim 4 is dependent on claim 1 and is believed to be allowable for at least the reasons claim 1 is allowable. In addition, claim 4 recites that the second silicided gate is fully silicided. Appellants note that claim 14 recites a similar feature. With respect to claim 4, the Final Office Action states that Fried in view of Wang discloses this feature, but points to no portion of either Fried or Wang for support (Final Office Action – page 3). Therefore, a prima facie case with respect to claim 4 has not been made. Appellants note the Final Office Action did not address a similar feature with respect to claim 14. In any event, neither Fried nor Wang discloses or suggests this feature.

For example, Fried discloses that a silicided gate conductor may include polysilicon with Nickel or Cobalt (Fried – col. 10, lines 4-6). Although this portion of Fried may disclose that a gate conductor may be silicided, this portion of Fried cannot be fairly construed to disclose or suggest that gate conductor 12 is fully silicided. That is, the term "fully silicided" is a conventional term in this art that indicates that the structure, (a gate structure in this case) is silicided throughout the entire structure. For example, Appellants' disclosure at paragraph 46 indicates that the term "fully silicided" represents that gate structure 700 is silicided down to dielectric cap 140 (See Fig. 7). Fried does not disclose a gate structure that is fully silicided.

Wang discloses that the gate structures in regions 1 and 2 are both partially silicided. That is, gate structures of the devices in regions 1 and 2 have different silicide thicknesses 15b and 15c, as illustrated in Fig. 7. Neither of the gate structures of Wang, however, is fully

silicided as clearly shown by the non-silicided portions 6 of the gate structures in Fig. 7.

Therefore, contrary to the assertion at page 3 of the Final Office Action, neither Fried nor Wang discloses or suggest that one of the gates is fully silicided, as required by claim 3.

Appellants note that Dash may disclose a platinum silicide gate electrode 50 that is formed by depositing a layer of platinum and reacting the platinum with polysilicon (Dash – col. 3, lines 50-57 and Fig. 8). It is not clear as to whether the entire structure of gate electrode 50 is silicided. Assuming for the sake of argument, however, that the entire structure of gate electrode 50 is silicided, Appellants submit that the Final Office Action has not provided any motivation as to why it would have been obvious to combine Dash with the combination of Fried and Wang. Accordingly, a prima facie case with respect to claim 4 should not include teachings from Dash. Further, Appellants assert that it would not have been obvious to combine Dash with Fried and Wang for reasons similar to those given above with respect to claim 1.

Therefore, Appellants respectfully submit that the rejection of claim 4 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claims 4, 5 and 14-18 is respectfully requested.

3. Claim 21

Claim 21 recites that a width of the first fin and the second fin ranges from about 10 Å to about 100 Å. The Final Office Action admits that Fried does not expressly disclose this feature (Final Office Action – page 5). The Final Office Action, however, states that Fried

discloses the width of the fin reaches a lower limit of 200 Å and points to col. 7, lines 55-56 for support (Final Office Action – page 6). Initially, Appellants note that Fried at col. 7, lines 55-56 discloses that the thickness of the fin ranges from 20 nm to 160 nm. The thickness of the fins, however, corresponds to the height of the fins, as disclosed at col. 7, lines 55-57 of Fried. Claim 21, in contrast, recites that the width of the first and second fins ranges from about 10Å to about 100Å. Fried is totally silent with respect to the width of fins 206. Appellants, therefore, assert that Fried cannot be fairly construed to disclose or suggest the claimed width since Fried provides no indication as to the width of fins 206.

Appellants note that the Final Office Action states that it would have been obvious to create a thinner fin since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum of workable ranges involves only routine skill in the art and points to In re Aller for support (Final Office Action – page 6). Appellants respectfully disagree.

As discussed above, rejections based on 35 U.S.C. § 103 must rest on a factual basis. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 177-78 (CCPA 1967). In making such a rejection, the Examiner has the initial duty of supplying the requisite factual basis and may not, because of doubts that the invention is patentable, resort to speculation, unfounded assumptions, or hindsight reconstruction to supply deficiencies in the factual basis. Id.

In the present case, the Examiner has not advanced any factual basis as to why it would have been obvious to modify Fried to read on the feature recited in claim 21. Instead the Examiner attempts to overcome the deficiencies in the combination of Fried and Wang by

resorting to so-called mechanical or per se rules of obviousness allegedly established by the Aller case. Such per se rules do not exist, however, and the reliance thereon by the Examiner to establish obviousness under 35 U.S.C. § 103 is improper. See In re Ochiai, 71 F.3d 1565, 1570, 37 USPQ2d 1127, 1132 (Fed. Cir. 1995); In re Wright, 343 F.2d 761, 769-70, 145 USPQ 182, 190 (CCPA 1965).

Therefore, Appellants respectfully submit that the imposed rejection of claim 21 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 21 is respectfully requested.

4. Claim 22

Claim 22 is dependent on claim 14 and is believed to be allowable for at least the reasons claim 14 is allowable. In addition, claim 22 recites a feature similar to claim 21. For reasons similar to those discussed above with respect to claim 21, Appellants respectfully submit that the imposed rejection of claim 22 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 22 is respectfully requested.

5. Claim 23

Claim 23 recites that a drain region of the first fin is electrically connected to a source region of the second fin. The Final Office Action states that Fried shows two drain regions connected together and those skilled in the art will recognize that "the appellations source and drain are interchangeable, simply designating the direction of current flowing through the

channel" (Final Office Action – page 6 at footnote 3). Appellants respectfully disagree.

While source and drain regions do indicate the flow of current through the channel, Fried clearly discloses that two drain regions 306 and 312 may be connected (Fried – col. 11, lines 64-67 and Fig. 9). Therefore, Appellants assert that modifying Fried to read on the feature recited in claim 23 amounts to more than merely changing names of the source/drain. That is, drain region 306 of transistor 302 in Fried would have to be connected to source region 310 of transistor 308. Fried, however, clearly does not disclose or suggest this as an alternate configuration to the configuration illustrated in Fig. 9, which clearly shows drain regions 306 and 312 being connected to each other.

Therefore, Appellants respectfully submit that the imposed rejection of claim 23 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 23 is respectfully requested.

B. Rejection under 35 U.S.C. § 103(a) based on Fried in view of Wang and further in view of Takeda

1. Claim 19

Claim 19 recites a third device formed on the insulating layer, including: a third fin formed on the insulating layer, a third dielectric layer formed on the third fin, and a partially silicided gate formed over a portion of the third fin and the third dielectric layer, wherein a silicided portion of the partially silicided gate formed over the portion of the third fin and the third dielectric layer has a different thickness than a silicided portion of the partially silicided

gate formed over the portion of the first fin and the first dielectric layer. The Final Office Action admits that neither Fried nor Wang discloses these features, but states that Takeda discloses these features and points to Fig. 3 of Takeda for support (Final Office Action – page 6). Appellants respectfully disagree.

Takeda at Fig. 3 illustrates a portion of a content addressable memory (CAM) having a number of memory cells (Takeda – page 1, paragraphs 5 and 14). It is not clear which portion of Takeda is alleged to disclose the claimed third device of claim 19, which includes a partially silicided gate formed over a portion of a third fin and a third dielectric layer, where a silicide portion of the partially silicided gate has a different thickness than a silicided portion of the partially silicided gate formed over a portion of the first fin and the first dielectric layer.

As best understood by Appellants, the silicided portions of the gate structures 5 in Fig. 3 of Takeda (i.e., the upper portions of the gate electrodes 5), all appear to have the same thickness. Claim 23, however, requires that a third partially silicided gate has a different thickness than a silicided portion of the silicided gate formed over the portion of the first fin and the first dielectric layer. Takeda does not disclose or suggest this feature.

In addition, assuming for the sake of argument, that Takeda could be fairly construed to disclose or suggest the claimed third device, Appellants assert that the motivation to combine Takeda with the combination of Fried and Wang does not satisfy the requirements of 35 U.S.C. § 103.

For example, the Final Office Action states that it would have been obvious to provide a third FinFET device "disclosed in the manner of Fried with a third thickness of silicide as

disclosed by Wang for the purpose, for example, of further diversifying the capabilities of the semiconductor device" (Final Office Action – page 6).

Appellants assert that such motivation does not even reference Takeda and provides no motivation for combining Takeda with the combination of Fried and Wang. Further, the alleged motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

Therefore, Appellants respectfully submit that the imposed rejection of claim 19 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 19 is respectfully requested.

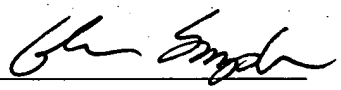
IX. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-7, 14-19 and 21-23.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 

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X. APPENDIX

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a first device formed on the insulating layer, including:

a first fin formed on the insulating layer, and

a first silicided gate formed over a portion of the first fin and including a first thickness of silicide material; and

a second device formed on the insulating layer, including:

a second fin formed on the insulating layer, and

a second silicided gate formed over a portion of the second fin and including a second thickness of silicide material different from the first thickness, wherein

a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.

2. The semiconductor device of claim 1, wherein the first device further includes:

a first dielectric layer formed between the first fin and the first silicided gate, and

wherein the second device further includes:

a second dielectric layer formed between the second fin and the second silicided gate.

3. The semiconductor device of claim 1, wherein the first silicided gate is partially silicided and the first thickness ranges from about 100 Å to about 500 Å.

4. The semiconductor device of claim 1, wherein the second silicided gate is fully silicided.

5. The semiconductor device of claim 4, wherein the second thickness ranges from about 400 Å to about 1000 Å.

6. The semiconductor device of claim 1, wherein the first device is an NMOS device and the second device is a PMOS device.

7. The semiconductor device of claim 1, wherein the first device and the second device are included in a single circuit element.

14. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a first device formed on the insulating layer, including:

a first fin formed on the insulating layer,

a first dielectric layer formed on the first fin, and

a partially silicided gate formed over a portion of the first fin and the first dielectric layer; and

a second device formed on the insulating layer, including:

a second fin formed on the insulating layer,

a second dielectric layer formed on the second fin, and

a fully silicided gate formed over a portion of the second fin and the second dielectric layer, wherein

a threshold voltage of the second device varies about 200 millivolts to about 400 millivolts from a threshold voltage of the first device.

15. The semiconductor device of claim 14, wherein a silicided portion of the partially silicided gate has a thickness ranging from about 100 Å to about 500 Å.

16. The semiconductor device of claim 14, wherein the fully silicided gate has a thickness ranging from about 400 Å to about 1000 Å.

17. The semiconductor device of claim 14, wherein one of the first device and the second device is an NMOS device and another one of the first device and the second device is a PMOS device.

18. The semiconductor device of claim 14, wherein the first fin and the second fin are

electrically connected.

19. The semiconductor device of claim 14, further comprising:

a third device formed on the insulating layer, including:

a third fin formed on the insulating layer,

a third dielectric layer formed on the third fin, and

a partially silicided gate formed over a portion of the third fin and the third dielectric layer, wherein

a silicided portion of the partially silicided gate formed over the portion of the third fin and the third dielectric layer has a different thickness than a silicided portion of the partially silicided gate formed over the portion of the first fin and the first dielectric layer.

21. The semiconductor device of claim 1, wherein:

a width of the first fin and the second fin ranges from about 10 Å to about 100 Å.

22. The semiconductor device of claim 14, wherein:

a width of the first fin and the second fin ranges from about 10 Å to about 100 Å.

23. The semiconductor device of claim 18, wherein a drain region of the first fin is electrically connected to a source region of the second fin.